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INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(51) International Patent Classification 5 :		(11) International Publication Number: WO 91/09422
H01L 23/485, 21/90	A1	(43) International Publication Date: 27 June 1991 (27.06.91)

(21) International Application Number: PCT/CA90/00448

(22) International Filing Date: 19 December 1990 (19.12.90)

(30) Priority data:
006,174 20 December 1989 (20.12.89) CA

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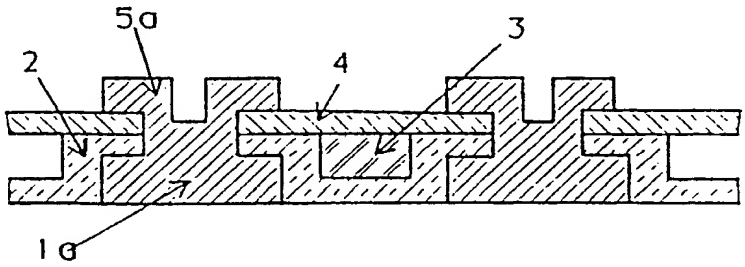
(81) Designated States: AT (European patent), BE (European patent), CH (European patent), DE (European patent), DK (European patent), ES (European patent), FR (European patent), GB, GB (European patent), GR (European patent), IT (European patent), JP, KR, LU (European patent), NL (European patent), SE (European patent), US.

Published
With international search report.
Before the expiration of the time limit for amending the claims and to be republished in the event of the receipt of amendments.

(54) Title: METHOD OF MAKING CRACK-FREE INSULATING FILMS WITH SOG INTERLAYER



(57) Abstract

A method of fabricating a semiconductor device is disclosed characterized in that a first dielectric layer is applied over an interconnect layer having tracks defining a conductive pattern, the first dielectric layer forming valleys between the tracks of the interconnect layer, spin-on glass is applied over said first layer to planarize it by forming spin-on glass zones in the valleys defined by the first dielectric layer, and a second layer is applied to the planarized first layer, whereby the first and second layers and said spin-on glass zones form a composite multi-layer film. The first layer is formed such that it has compressive stress at room temperature to prevent cracking in the composite multi-layer film during subsequent heat treatment. The second layer can be another dielectric layer or a further interconnect layer applied directly to the first layer and SOG planarization layer. The method can also be applied to other fields, such as the manufacture of optical fibers, emission diodes and the like.

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METHOD OF MAKING CRACK-FREE INSULATING FILMS WITH SOG INTERLAYER

This invention relates to method of making crack-free insulating films comprising a Spin-on glass (SOG) layer, and insulating films made thereby.

Spin-on glasses (SOG) are proprietary liquid solutions containing siloxane or silicate based monomers diluted in various kinds of solvents or alcohols. During coating and curing, monomers are polymerized by condensation and release water, solvent, and alcohol. The condensed material is a thin solid film having mechanical, chemical and electrical properties which depend on the starting composition, and the coating and curing process. A good starting solution can give bad results if the coating and curing sequence is not optimized.

There are more than one hundred different SOG solutions on the market. They are classified into two major families:

1) Siloxanes (methyl-, ethyl-, phenyl-, butyl-, doped or undoped).

2) Silicates (doped or undoped).

Planarization is the filling in of the trenches and crevices formed when a plurality of layers, some of which might be subsequently etched back, are deposited on a substrate. Planarization is used over polysilicon, refractory metals, polycides, silicides, aluminum and aluminum alloys, copper, and gold or otehr conductive materials. The main goal is to smooth/eliminate steps and enhance step coverage by the dielectrics and interconnects. Planarization technology becomes increasingly important when the scale of integrated circuits is in the micron and submicron region. Of the many dielectric planarization

techniques, SOG planarization is a particularly attractive method; it is relatively simple, economical and is capable of high throughput.

Unfortunately, the purely inorganic silicate SOGs are prone to cracking. This has limited their usefulness in semiconductor and similar applications, especially where they have to undergo subsequent heat treatment. While the quasi-inorganic siloxane SOGs have a more flexible structure due to the presence of organic radicals, which prevent complete cross-linking of the $SiO_xC_yH_z$ matrix under condensation, the organic radicals are not stable at high temperatures and are not compatible with oxygen plasma photoresist strippers (which tend to transform the quasi-inorganic SOG to a purely inorganic SOG by burning the organic bonds and producing volatile species like H_2O, $C_xO_yH_z$, and silanol Si-OH). These two drawbacks, among others, limit the use of the quasi-inorganic siloxanes as an alternative to the silicates.

SOG planarization can take three forms:

1) Complete etchback.
2) Partial etchback.
3) Non etchback.

Total etchback and partial etchback processes for planarization of dielectrics over aluminum use photoresist, polyimide, or flexible quasi-inorganic SOGs. In those two cases, cracking of the dielectric sandwich does not occur since most of the planarizing material is removed from the wafer.

Major manufacturing restrictions of the complete/partial etchback techniques impose the non-etchback approach as the preferred technique in a production environment. In this approach, the SOG becomes

a permanent part of the dielectric. Non-etchback silicate SOG planarization of dielectrics over polysilicon, polycides, refractory metals or silicides has been used for about three years. This technique is not particularly demanding on the dielectric sandwich because the coefficient of thermal expansion of the materials is much lower than for aluminum and aluminum alloys. The dielectric sandwich does not normally crack over those materials.

Non-etchback SOG planarization of dielectrics over aluminum alloys is an extremely new process in the semiconductor industry. Unfortunately, purely inorganic SOG form dielectric sandwiches which are prone to very bad cracking. Consequently, more flexible quasi-organic SOGs have been tried, but this approach has proved to be questionable because of a serious field inversion problem due to the effect of the hydrogen contained in the organic bonds of the quasi-inorganic SOGs on the characteristics of CMOS semiconductor devices.

SOG film properties are of prime importance. Since SOG is generally a more porous material, when compared to LPCVD, APCVD, LACVD, PACVD or PECVD oxides, it is more prone to water absorption. This water absorption reduces the bulk resistivity of the SOG and increases the power consumption of the semiconductor device due to current leakage between adjacent tracks of interconnect. For this reason, among others, SOG must not come into direct contact with the tracks and must be sandwiched between two denser LPCVD, APCVD, LACVD, PACVD or PECVD dielectric films.

Interconnections between upper and lower tracks by the use of contacts or vias are necessary, and the SOG is then in direct contact with the interconnects at those locations. If too much water is present in the SOG (or if water is generated in the quasi-inorganic SOG during

photoresist stripping, after vias/contact patterning), problems such as via poisoning can occur. One way to prevent via poisoning is to use a dense and purely inorganic SOG, which is not degraded by photoresist strippers. For this reason as well silicate SOGs are preferred, but the formation of microcracks discussed above, especially during subsequent heat treatments, has limited their usefulness.

It has previously been thought that the formation of microcracks in the inorganic SOG layer was an unavoidable consequence of the brittle nature of the SOG material. For example. Japanese patent publication no. 63-021837 seeks to avoid the cracking that occurs in the SOG film during the vitrifying step by coating with SOG under reduced pressure. JP 62-046533 seeks to avoid cracking in the SOG film by pressing the SOG solution with a heating plate during solidification of the SOG layer. There has thus been a tendency to abandon altogether SOGs for planarization purposes despite their otherwise attractive properties in terms of simplicity, economy and high throughput.

It has now been discovered in accordance with the invention that the cracking that occurs in insulating films with SOG planarization interlayers is not mainly due to cracking in the SOG layer, as previously thought, but rather primarily due to the different coefficients of expansion of the SOG, dielectric layers, and interconnect materials.

Accordingly the present invention provides in a method of fabricating a composite insulating film comprising first and second layers with intermediate spin-on glass zones acting as a planarization interlayer for said first layer, at least said first layer being a dielectric layer, the improvement wherein the first layer is formed under

compression to prevent cracking in the composite film during subsequent heat treatment.

The second layer can either be a second dielectric layer, or where, in the case of semiconductor fabrication, an interconnect layer is applied directly over the first and SOG layers, the second layer can be the interconnect layer.

The method may be applied to the fabrication of a semiconductor device wherein a first dielectric layer is applied over an interconnect layer having tracks defining a conductive pattern and made of material having a high coefficient of expansion, the first dielectric layer forming valleys between the tracks of the interconnect layer, spin-on glass is applied over said first layer to planarize it by forming spin-on glass zones in the valleys defined by the first dielectric layer, and a second layer is applied to the planarized first layer, whereby said first and second layers and said spin-on glass zones form a composite multi-layer film.

In the above method the first layer is formed under compression to prevent cracking in the composite multi-layer film during subsequent heat treatment.

The invention will now be described in more detail, by way of example only, with reference to the accompanying drawings in which:-

Figures 1a to 1h illustrate the steps in the manufacture of a composite insulating film with a SOG interlayer.

First a layer of aluminum interconnect material 1 (Fig. 1a) is deposited on a substrate and then patterned using photolithography (Fig. 1b). A first layer of

dielectric 2 is deposited over the etched interconnect tracks (Fig. 1c) and a an inorganic (silicate) spin-on glass (SOG) layer 3 is applied (with or without etchback) to fill the valleys and crevices (Fig. 1d). The SOG is a proprietary composition and can be obtained from a number of sources such as Allied Signal Inc, Milpitas, California. Being liquid, the SOG is almost absent over the peaks 1a and provides good planarization for the first dielectric layer 2.

A second dielectric layer 4 is then applied over the first layer 2 and SOG interlayer 3 (Fig. 1e). Contacts holes are then etched away to reach the tracks of the first layer of interconnect material 1 (fig. 1f). A second level of interconnect material 5 is deposited over the etched second layer 4 (fig 1f) and is patterned using photolithography to form the desired conductive tracks 5a (Fig. 1h).

Such dielectric sandwiches containing dense purely inorganic (silicate) SOG crack during the subsequenet heat treatments which are needed to cure and stabilize the SOG and the aluminum alloys.

These cracks in the dielectric sandwiches cause the device to fail due to electrical shorts between adjacent tracks of the same level of interconnect (intralevel short), or between tracks of two independent levels of interconnect (interlevel shorts). This property has limited the use of the purely inorganic SOGs (silicates) and some quasi-inorganic SOGs (siloxanes) for dielectric planarization applications.

Thin film stress can be compressive or tensile. A compressive stress, when too excessive, results in delamination, formation of waves and ripples. A film in compression does not crack. In fact, a film in compression

stops the propagation of cracks. A tensile stress, when too excessive, results in crack formation and propagation.

When a stressed film is deposited on a substrate, it induces a mechanical bow of that substrate. The bow direction and its magnitude is related to the stress type (tensile or compressive), and its intensity. If the film is in tension, the substrate bows in such a way that the film is present on the concave face. Similarly, if the film is under compression the substrate bows in such a way that the film is present on the convex face. The stress nature of a given thin film can then be measured by the change of curvature induced in a (100) Si single crystal wafer, due to the deposited film.

Using a laser optical lever, the wafer can be scanned before and after the deposition to obtain the net change or wafer radius of curvature. The film stress "σ" is calculated using the following expression:

$$\sigma = [Et^2]/[6(1-\pi)r\tau]$$

where "E" is the Young's modulus of Si (100) wafer, "π" is its Poisson's ratio, "t" is the wafer thickness, "r" is the measured net radius of curvature, and "τ" is the film thickness.

Such stress measurements have been performed on various purely inorganic (silicates) SOGs. A (6-8) x 10^8 dyne/cm^2 tensile stress was measured. This tensile stress is the result of the solid phase volumetric shrink of the SOG during its condensation:

$$SiO_t(OC_2H_5)_u(OH)_v + wH_2O \rightarrow SiO_xH_y + zH_2O + bC_2H_5OH$$

Water (H_2O) and ethanol (C_2H_5OH) by-products are released and contribute to an increase of the internal stress.

The SOG stress obtained is not excessively high but the obtained material is very rigid. Although it was not possible to measure the actual coefficient of thermal expansion of the obtained SOG, the appearance of cracks at high temperature in the dielectric sandwich PSG/SOG/PSG (PSG stands for a 4.0 wt% phosphorus doped LPCVD SiO_2 film which is under a tensile stress of 0.5 - 3.0 x 10^9 dyne/cm^2, up to four times higher than SOG), deposited over metal tracks of the first level of interconnect, and the absence of cracks in the dielectric sandwich PSG/PSG deposited over equivalent metal tracks, indicates that the SOG has a much smaller coefficient of thermal expansion than PSG.

It is not, as previously thought, a high stress in the SOG which causes the appearance of cracks, but rather its lower coefficient of thermal expansion. The cracks appear in the dielectric sandwich around and over the metal I tracks and propagate easily through the dielectric layers, which are already in tensile stress. Since aluminum inherently has a very high coefficient of thermal expansion, when compared to PSG and particularly SOG, the problem is important, especially in view of the subsequent heat treatments that are required.

In accordance with the invention, the dielectric sandwich cracking has been substantially eliminated with a special combination of film stresses.

The first dielectric layer 1 deposited over the aluminum and under the SOG film must be under compressive stress. In this case, the heat treatments that cause expansion of the aluminum will tend to bring the dielectric

under tension. But since the dielectric is already in compression, its stress will stabilize at an almost negligible value. A stress of about 5×10^8 to 3×10^9 dyne/cm^2 is preferred and its exact value depends on the difference of the coefficient of thermal expansion between the aluminum alloy and the dielectrics used in the sandwich.

The SOG layer has a stress that is slightly tensile at about $6 - 8 \times 10^8$ dynes/cm^2. The last dielectric layer 4 deposited over the SOG layer 3 and under the second interconnect layer 5 can be under compressive or tensile stress, but a tensile stress is preferred to compensate for the wafer bow generated by the first dielectric. A stress of about 5×10^8 to 3×10^9 dyne/cm^2 is preferred.

Stress measurements have been performed on various different dielectrics to find one that has the required compressive stress. A specially designed undoped LPCVD SiO_xH_v (SG) gives the desired behaviour, namely a compressive stress of 2×10^9 dyne/cm^2. A sandwich composed of 600 nm SG/200 nm SOG/600 nm PSG can theoretically be crack free.

Example

An experiment was performed to compare a standard PSG/SOG/PSG sandwich with a SG/SOG/PSG sandwich fabricated in accordance with the invention. For the experiment, an equal number of blanket aluminum deposited wafers and real patterned device wafers were used to deposit 600 nm of PSG or 600 nm of the special SG. Then, all the wafers were coated with SOG and heat treated. Finally, another 600 nm of PSG was deposited on the top of the SOG, and heat treatments were performed to check for cracking.

All wafers with PSG/SOG/PSG sandwich were badly cracked. The PSG/SOG/PSG covered blanket aluminum deposited silicon wafers were randomly cracked. The PSG/SOG/PSG covered wafers with patterns showed cracks that were limited to the area over the aluminum lines of the first level of interconnect, indicating that the coefficient of thermal expansion of SOG is really the underlying cause of the dielectric sandwich cracking.

All wafers with SG/SOG/PSG sandwich were completely crack-free. Even the SG/SOG/PSG covered blanket aluminum deposited silicon wafers were absolutely crack-free. This proves the effectiveness of having a compressive pre-stressed film under the SOG to compensate for its low coefficient of thermal expansion.

The described method is very important because it permits a non-etchback high quality purely inorganic SOG process to be applied to high coefficient of thermal expansion materials, such as aluminum alloys.

There are a number of ways of achieving the desired compressive stress. Examples are as follows:

- Low Pressure Chemical Vapour Deposition (LPCVD)
- Plasma Enhanced Chemical Vapour Deposition (PECVD)
- Laser Assisted Chemical Vapour Deposition (LACVD)
- Photochemical Chemical Vapour Deposition (PhCVD)
- Atmospheric Pressure Chemical Vapour Deposition (APCVD)
- Bias Sputtering (BS)
- Thermal oxidation
- Spin-on deposition
- Electron Cyclotron Resonance (ECR), biased or otherwise.

The deposited compressive material under the SOG can be:

- Silicon nitride, stochiometric or not, with or without H, Cl, F
- Polyimide or other mechanically deposited organic dielectric
- Silicon dioxide, oxynitride, stochiometric or not, with or without H, Cl, F
- Above-mentioned materials doped/alloyed with As, P, B,

  Pb, or other metallic elements, or their combinations.

The layer 4 over the SOG layer 3 need not be under tension but also can be under compression.

The SOG can be of many types. The crack prevention effect is much more pronounced with low coefficient of thermal expansion inorganic (silicates) SOGs.

The interconnect material under the SOG can be other than aluminum or aluminum alloy. For example, it can be a metal such as W, Mo, Ta, Co, Ti; or a reacted metal such as Ti_xN_y, Ti_xW_y, $Ti_xO_vZ_z$, $Ti_xW_vN_z$. It can also be a silicide of W, Mo, Ta, Co, Ti, Pt.

The upper part of the dielectric sandwich can be omitted and the second metal layer 5 directly deposited over the SOG layer 3 and first dielectric layer 2.

The described process has many applications. In particular, it can be applied to other steps in the manufacture of integrated circuits, such as:

- Planarization
- Diffusion source

- Dielectric layer
- Diffusion barrier
- Encapsulation
- Adhesion layer
- Buffer layer
- Antireflective layer
- Corrosion protection layer Etc.

It can also be applied to other semiconductor devices, such as:

- Emission diodes
- Liquid crystal displays
- Electro chromic displays
- Photodetectors
- Solar batteries
- Sensors

In other fields, the process may be useful in the fabrication of:

- Optical fibers
- Corrosion protection
- Adhesion promoters
- Friction reduction coatings
- Optical/thermal reflectance adjustment coatings

Claims

1. A method of fabricating a composite insulating film comprising first and second layers with intermediate spin-on glass zones acting as a planarization SOG interlayer for said first layer, at least said first layer being a dielectric layer, characterized in that the first layer is formed under compression to prevent cracking in the composite film during subsequent heat treatment.

2. A method as claimed in claim 1, characterized in that said first layer is formed under a compressive stress of about 5×10^8 to 5×10^9 dynes/cm^2.

3. A method as claimed in claim 2, characterized in that said SOG interlayer is formed under a slightly tensile stress of about 3×10^8 dynes/cm^2.

4. A method as claimed in claim 3, characterized in that said second layer is formed under a compressive stress of about 5×10^8 to 5×10^9 dynes/cm^2.

5. A method as claimed in claim 4, characterized in that said first layer comprises siO_xH_y (SG).

6. A method as claimed in claim 5, characterized in that said second layer comprises PSG.

7. A method as claimed in claim 6, characterized in that said first layer and/or second layer is deposited by LPCVD (Low Pressure Chemical Vapour Deposition).

8. A method as claimed in claim 6, characterized in that said first layer and/or second layer is deposited by Plasma Enhanced Chemical Vapour Deposition (PECVD).

9. A method as claimed in claim 6, characterized in that said first layer and/or second layer is deposited by Laser Assisted Chemical Vapour Deposition (LACVD).

10. A method as claimed in claim 6, characterized in that said first layer and/or second layer is deposited by Photochemical Chemical Vapour Deposition (PhCVD).

11. A method as claimed in claim 6, characterized in that said first layer and/or second layer is deposited by Atmospheric Pressure Chemical Vapour Deposition (APCVD).

12. A method as claimed in claim 6, characterized in that said first layer is deposited by Bias Sputtering (BS).

13. A method as claimed in claim 6, characterized in that said first layer and/or second layer is deposited by Spin-on deposition.

14. A method as claimed in claim 6, characterized in that said first layer and/or second layer is deposited by Electron Cyclotron Resonance (ECR), biased or otherwise.

15. A method as claimed in claim 4, characterized in that said first layer and/or second layer comprises silicon nitride, stochiometric or not, with or without H, Cl, F.

16. A method as claimed in claim 4, characterized in that said first layer and/or second layer comprises polyimide or other mechanically deposited organic dielectric.

17. A method as claimed in claim 4, characterized in that said first layer and/or second layer comprises silicon dioxide, oxynitride, stochiometric or otherwise, with or without H, Cl, F.

18. A method as claimed in claim 4, characterized in that said first layer and/or second layer comprises materials as claimed in any of claims 15 to 18 doped/alloyed with As, P, B, Pb, or other metallic elements, combinations thereof.

19. A method of fabricating a semiconductor device characterized in that a first dielectric layer is applied over an interconnect layer having tracks defining a conductive pattern and made of material having a high coefficient of expansion, the first dielectric layer forming valleys between the tracks of the interconnect layer, spin-on glass is applied over said first layer to planarize it by forming spin-on glass zones in the valleys defined by the first dielectric layer, and a second layer is applied to the planarized first layer, whereby said first and second layers and said spin-on glass zones form a composite multi-layer film, characterized in that said first layer is formed under compression to prevent cracking in the composite multi-layer film during subsequent heat treatment.

20. A method as claimed in claim 19, characterized in that said second layer is a dielectric layer.

21. A method as claimed in claim 19, characterized in that said second layer is an interconnect layer deposited directly onto said first layer planarized with said SOG interlayer.

22. A method as claimed in claim 19, characterized in that said SOG interlayer is formed under a slightly tensile stress of about 5×10^8 dynes/cm^2.

23. A method as claimed in claim 22, characterized in that said second layer is formed under a compressive stress of about 5×10^8 to 3×10^9 dynes/cm^2.

24. A method as claimed in claim 23, characterized in that said first layer comprises SiO_xH_y (SG).

25. A method as claimed in claim 23, characterized in that said second layer comprises PSG.

26. A method as claimed in claim 25, characterized in that said first layer is deposited by LPCVD (Low Pressure Chemical Vapour Deposition).

27. A method as claimed in claim 25, characterized in that said first layer is deposited by Plasma Enhanced Chemical Vapour Deposition (PECVD).

28. A method as claimed in claim 19, characterized in that said tracks are made of aluminum or aluminum alloy.

29. A method as claimed in claim 19, characterized in that said tracks are made of material selected from the group consisting of: W, Mo, Ta, Co, Ti; or a reacted metal such as Ti_xN_y, Ti_xW_y, $Ti_xO_vZ_z$, $Ti_xW_vN_z$; or a silicide of W, Mo, Ta, Co, Ti, Pt.

30. A composite insulating film comprising first and second layers with intermediate spin-on glass zones acting as a planarization SOG interlayer for said first layer, at least said first layer being a dielectric layer, characterized in that the first layer is formed under compression to prevent cracking in the composite structure during subsequent heat treatment.

31. A composite insulating film as claimed in claim 30, characterized in that said first layer comprises SiO_xH_y (SG).

32. A composite insulating film as claimed in claim 30, characterized in that said first layer comprises

silicon nitride, stochiometric or otherwise, with or without H, Cl, F.

33. A composite insulating film as claimed in claim 30, characterized in that said first layer comprises polyimide or other mechanically deposited organic dielectric.

34. A composite insulating film as claimed in claim 30, characterized in that said first layer comprises silicon dioxide, oxynitride, stochiometry otherwise, with or without H, Cl, F.

35. A composite insulating film as claimed in claim 30, characterized in that said first layer comprises materials as claimed in any of claims 31 doped/alloyed with As, P, B, Pb, or other metallic elements, combinations thereof.

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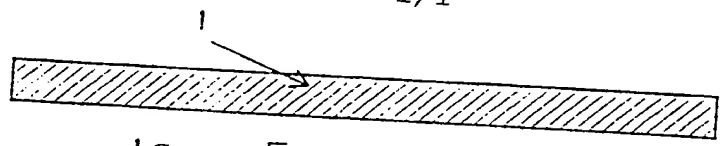

Fig. 1a

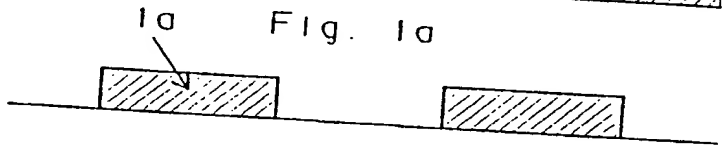

Fig. 1b

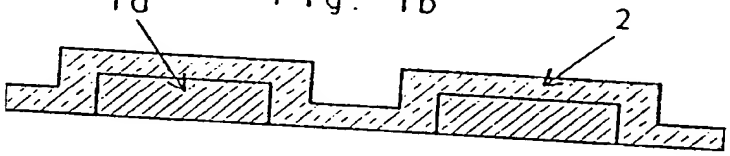

Fig. 1c

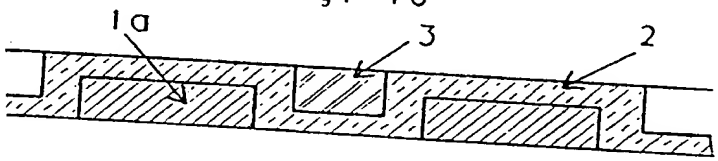

Fig. 1d

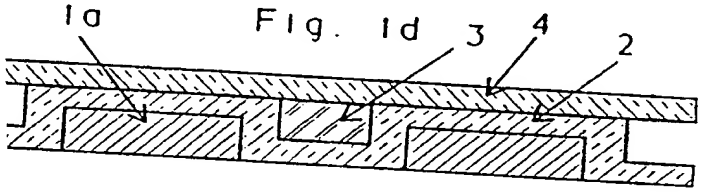

Fig. 1e

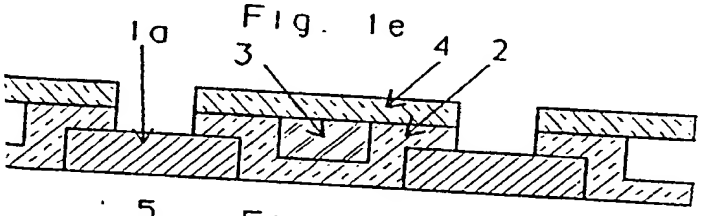

Fig. 1f

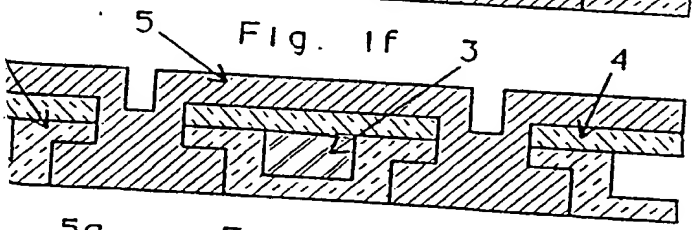

Fig. 1g

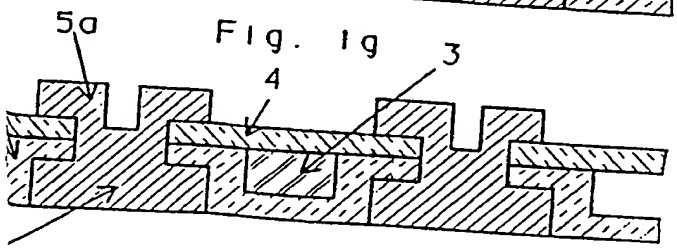

Fig. 1h

ANNEX TO THE INTERNATIONAL SEARCH REPORT ON INTERNATIONAL PATENT APPLICATION NO.

CA 9000448
SA 42807

This annex lists the patent family members relating to the patent documents cited in the above-mentioned international search report.
The members are as contained in the European Patent Office EDP file on 22/04/91
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EP-A-46059	17-02-82	JP-C- 1400232	28-09-87
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		US-A- 4394401	19-07-83

INTERNATIONAL SEARCH REPORT

International Application No PCT/CA 90/00448

I. CLASSIFICATION OF SUBJECT MATTER (if several classification symbols apply, indicate all)[6]

According to International Patent Classification (IPC) or to both National Classification and IPC

Int.Cl. 5 H01L23/485 ; H01L21/90

II. FIELDS SEARCHED

Minimum Documentation Searched[7]

Classification System	Classification Symbols
Int.Cl. 5	H01L21

Documentation Searched other than Minimum Documentation to the Extent that such Documents are Included in the Fields Searched[8]

III. DOCUMENTS CONSIDERED TO BE RELEVANT[9]

Category °	Citation of Document, [11] with indication, where appropriate, of the relevant passages [12]	Relevant to Claim No.[13]
A	WO,A,8702828 (MOTOROLA) 07 May 1987 see abstract	1, 19, 30
A	EP,A,46059 (FUJITSU) 17 February 1982 see page 6, line 31 - page 7, line 12	1, 19, 30

° Special categories of cited documents : [10]

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier document but published on or after the international filing date

"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

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"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art.

"&" document member of the same patent family

IV. CERTIFICATION

Date of the Actual Completion of the International Search	Date of Mailing of this International Search Report
22 APRIL 1991	16 MAY 1991
International Searching Authority	**Signature of Authorized Officer**
EUROPEAN PATENT OFFICE	PHEASANT N.J. N.J. Pheasant